REMARKS

Claims 1-30 are pending. Claims 1-30 were rejected in the Office action dated February 20, 2008. Reconsideration of all rejected claims is requested in light of the amendments and arguments presented here.

Claim Rejections Under 35 U.S.C. §103

Claims 1, 7, 11, 15, 18, 22, 29, and 30 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,829,629 to Magesacher et al. ("Magesacher") in view of U.S. Patent No. 6,970,511 to Barnette ("Barnette").

Claim 1 recites, "a delay section comprising… a plurality of delay elements connected in series between the delay section input and the delay section output." The Office action acknowledged that these features were not shown by Magesacher, and cited Barnette instead. However, the cited motivation to combine the references is counter to the reference teachings and the references teach away from such a combination.

The Office action indicated that one would be motivated to replace the single delay stage of Magesacher by the multiple delay stages of Barnette, "for the benefit of being able to specifically control sampling delay time, as each delay element delays the input signal by one sample delay," Office action, page 4, lines 1-3. However, Magesacher discloses, "Each signal path has a delay stage with a delay which can be set to different values…" column 2, lines 17-18 (emphasis added). Thus, replacing the variable delay stage of Magesacher with a plurality of stages of Barnette (each apparently providing a fixed delay) would not provide a benefit in controlling delay time, but would appear to provide less flexibility in controlling delay time by limiting delay time to some integer number of sample delays. "[F]irst, second, third, fourth and fifth first-signal delay stages… each delay the single-bit input signal by one sample delay." Column 15, lines 64-67. Thus, the cited motivation is counter to the reference teaching and does not provide a rationale for combining the references.

Furthermore, replacing a single delay stage with a plurality of delay stages would generally use additional area and Barnette teaches that using significant die area is problematic. "Such hardware multipliers consume significant electrical power and require significant die area

on an integrated circuit chip making such an approach problematic with a design criteria of low power and size." Column 3, lines 64-67 (emphasis added). Thus, Barnette teaches the importance of limiting area consumption and thereby teaches away from replacing a single component with multiple components in the manner proposed in the Office action.

In addition, Barnette teaches away from filter-based systems such as that of Magesacher, because Barnette teaches that such systems use excessive space. "Use of polyphase low-pass filter structure typically requires a read-only memory or a random access memory for coefficient storage, which adds significant area to the hardware." Column 4, lines 10-13.

Claims 2-14 depend from claim 1 and are submitted to be allowable at least for depending from an allowable base claim. Furthermore, claims 2-14 recite additional elements that further distinguish over the cited references.

For example, claim 5 as amended recites, "the plurality of delay elements comprises at least M delay elements, the plurality of delay elements delaying each of the M channel's data and providing an output that is specific to an individual channel of the M channels." Support for this amendment is found throughout the specification, for example in FIGs. 4A-4C and related text at page 12, line 1 – page 14, line 30. In particular, the specification discloses, "The delay elements 432 in the delay sections 430 delay each channel's data by a time period sufficient to process each channel's data separately and in sequence in integrator unit 420... The output of each delay section 430 is therefore data specific to each input channel." Page 14, lines 1-7. In contrast, the Magesacher and Barnette each appear to perform operations on single channels (e.g. input signals Rin0, Rin1, Rin2 of FIG. 5 of Barnette, and input Xi of FIG. 1 of Magesacher) and do not appear to delay each of M channel's data.

Claim 6 as amended recites, "a multiplexer that multiplexes M channels and provides a multiplexed signal to the integrator." Support for this amendment is provided throughout the specification, for example in FIGs. 4A-4C and related text. No such multiplexer appears to be shown in either reference. Both references appear to perform operations on single channels (e.g. input signals Rin0, Rin1, Rin2 of FIG. 5 of Barnette, and input Xi of FIG. 1 of Magesacher) and do not appear to multiplex signals, or otherwise provide an M channel decimator of claim 6.

Independent claims 15, 29, and 30 each recite, "a delay section comprising... a plurality of delay elements." Independent claims 26, 27, and 28 each recite, "a delay section comprising...

M delay elements," and "M>1." As discussed with respect to claim 1, these features are not taught or suggested by the cited references. Therefore, claims 15, 26, 27, 28, and 29 are submitted to be allowable.

Dependent claims 16-25 depend from claim 15 and are therefore submitted to be allowable at least for depending from an allowable base claim. Furthermore, claims 16-25 recite additional elements that have not been shown in the references.

Claims 13, 14, 24, and 25 were rejected under 35 U.S.C. §103(a) as being unpatentable over to Magesacher and Barnette as applied to claims 1 and 15 above, and further in view of U.S. Patent No. 4,999,798 to McCaslin et al. ("McCaslin"). However, McCaslin does not cure the defects in the rejections of claims 1 and 15 discussed above and thus these claims are allowable at least for depending from allowable base claims.

Claims 2-6, 8-10, 12, 16, 17, 19, 20, 21, and 23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Magesacher in view of Barnette and further in view of Applicant admitted prior art ("AAPA"). However, "AAPA" does not cure the defects in the rejections of claims 1 and 15 discussed above and thus these claims are allowable at least for depending from allowable base claims. Furthermore, to the extent that the rejection is based on treating material as admitted prior art because it is described in the background section, it is submitted that the background may contain material that is not prior art for all purposes and no admission is made with respect to any characterization of background material as prior art.

Claims 26-28 were rejected under 35 U.S.C. §103(a) as being unpatentable over Magesacher in view of Barnette and "AAPA," and further in view of McCaslin. Claim 26 recites, "an integrator section input comprising a multiplexer comprising M multiplexer inputs and a multiplexer output." No such integrator section input is shown in any of the four cited references. In particular, the Office action acknowledged that Magesacher, Barnette, and "AAPA" do not show such a multiplexer, and cited McCaslin instead. However, FIG. 2 of McCaslin shows no multiplexer at an input of integrator 12. Multiplexer circuit 18 is shown between differentiator 16 and interpolation circuit 22. There is no apparent reason to modify the reference by moving such a multiplexer circuit to integrator 12. In particular, it is noted that integrator 12 has a single input, not multiple inputs. Furthermore, multiplexer circuit 18 receives two inputs and provides two outputs, simply passing through, or swapping the two inputs. "Therefore, multiplexer circuit 18

is simply a means to swap back and forth the first and second outputs of differentiator circuit 16..." Column 5, lines 25-26. Thus, multiplexer circuit 18 does not appear to multiplex multiple inputs to provide a multiplexer output. Therefore, the features of claim 26 are not shown by the cited references.

Claims 27 and 28 also recite limitations regarding multiplexers that are not shown in the cited references. To the extent that the rejections of claims 27 and 28 are for the same reasons as claim 26, it is pointed out that claims 27 and 28 both recite different components (e.g. "a differentiator section input comprising a multiplexer" of claim 27, and "an oscillator input comprising a multiplexer" of claim 28) and thus it is not seen how they can be rejected on the same basis. Clarification is requested.

Information Disclosure Statement

A Supplemental Information Disclosure Statement is being filed herewith. It is respectfully requested that this Supplemental Information Disclosure Statement be considered and the PTO Form 1449 be initialed and returned with the next Action.

CONCLUSION

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. Should the Examiner believe that a telephone conference would expedite the prosecution of this application; the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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